REMARKS

Claims 1-12 and 14 are pending in the application. Claims 1, 6, and 8 have been amended hereby. Claims 1, 4, 6, 7, 8, and 11 are in independent form. Favorable reconsideration is requested.

Reconsideration is respectfully requested of the rejection of Claims 1-5, 8-12, and 14 under 35 U.S.C. §102(b), as being anticipated by Japanese Patent Publication No. H09-231093 ("Goettsu"); and of the rejection of Claims 6 and 7 under 35 U.S.C. §103(a), as being obvious over Goettsu in view of U.S. Patent No. 5,706,478 ("Dye").

In Goettsu, as best understood, the apparatus includes two CPUs which have different architecture from each other, and Goettsu discloses how the parameter is transmitted between the CPU's. For example, when Power PC code performed by the CPU having Power PC architecture calls X86 code performed by the CPU having X86 architecture, the return address having 64 bits is divided into two parts, each having 32 bits since the stack of X86 has 32 bits.

This feature of Goettsu is quite different from that of the presently claimed invention, as recited in amended independent Claims 1, 6, and 8. In the presently claimed invention, the first processor (GPU) performs both a main routine and a subroutine called by the main routine. The second processor only helps the call and return process executed inside the first processor, and does not perform the main routine or the subroutine. For this reason, the interrupt signal is necessary to request for help. See paragraph [0037] of the present application, for example. Since the process performed in Goettsu is a conventional function call, the interrupt signal is not necessary.

Further, in the presently claimed invention, as recited in independent Claims 4, 7, and 11, the call destination address is stored in formats of the call instruction and the accompanying

execution stop instruction dividedly. That is, the address is dividedly stored in two instruction codes regardless of which instruction the processors execute. The second processor only extracts the address to help the first processor to execute a call instruction. The same holds for the jump destination address.

In Goettsu, the return address is stored in the stack only when a call instruction is executed as mentioned above. This is a general function call process. The Office Action alleges that the Power PC executes a call instruction, the destination address and return address are 64 bits and are stored in two parts by the x86 system in Goettsu (pages 4 and 5 in the Office Action). However, it is respectfully submitted that there is no description about the destination address in Goettsu. This is because the Power PC itself executes the call instruction, therefore there is no need to divide the destination address.

Dye fails to cure the deficiencies of Goettsu.

Accordingly, it is respectfully submitted that independent Claims 1, 4, 6, 7, 8, and 11, and the claims depending therefrom, are patentably distinct over the cited references, alone or in any possible combination.

In view of the amendments and remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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